WHAT IS CLAIMED IS:

1. A test interface for providing test access by synchronous test equipment to an asynchronous circuit, the test interface comprising:

synchronous-to-asynchronous (S2A) conversion circuitry operable to receive synchronous input data serially from the synchronous test equipment and convert the synchronous input data to asynchronous input data;

asynchronous logic operable to transmit the asynchronous input data to a first test register in the asynchronous circuit, and to transmit asynchronous output data received from a second test register in the asynchronous circuit, the asynchronous output data resulting from application of the asynchronous input data to the asynchronous circuit, operation of the asynchronous logic being synchronized at least in part with a clock signal associated with the synchronous test equipment; and

asynchronous-to-synchronous (A2S) conversion circuitry operable to receive the asynchronous output data from the asynchronous logic, convert the asynchronous output data to synchronous output data, and serially transmit the synchronous output data to the synchronous test equipment.

2. The test interface of claim 1 wherein the asynchronous logic comprises a shift register which is operable alternately to receive the asynchronous input data serially from the S2A conversion circuitry and transmit the asynchronous output data serially to the A2S conversion circuitry.

3. The test interface of claim 2 wherein the asynchronous logic further comprises a parallel-to-serial (P2S) register operable to receive the asynchronous input data

in parallel from the shift register, and transmit the asynchronous input data serially to the first test register.

4. The test interface of claim 3 further comprising a serial tree interface coupled to the P2S register operable to transmit the asynchronous input data to the first test register.

5. The test interface of claim 2 wherein the asynchronous logic further comprises a serial-to-parallel (S2P) register operable to receive the asynchronous output data serially from the second test register, and transmit the asynchronous output data in parallel to the shift register.

6. The test interface of claim 5 further comprising a serial tree interface coupled to the S2P register operable to transmit the asynchronous output data from the second test register.

7. The test interface of claim 2 further comprising an interface controller operable to control operation of the asynchronous logic in accordance with the clock signal.

8. The test interface of claim 7 wherein the interface controller comprises a finite state machine having a plurality of associated states.

9. The test interface of claim 8 wherein selected ones of the plurality of states correspond to operations of the shift register, the shift register operations including a shift operation for shifting in the asynchronous input data and shifting out the asynchronous output data, an update operation for transmitting the asynchronous input data to the first test

register, and a capture operation for receiving the asynchronous output data from the second test register.

10. The test interface of claim 2 wherein the shift register is operable to perform a plurality of operations including a shift operation for shifting in the asynchronous input data and shifting out the asynchronous output data, an update operation for transmitting the asynchronous input data to the first test register, and a capture operation for receiving the asynchronous output data from the second test register.

11. The test interface of claim 10 the shift register is further operable to begin early shifting out of the asynchronous output data upon reception of the asynchronous output data and before commencement of a subsequent shift operation.

12. The test interface of claim 11 wherein the early shifting and the subsequent shift operation result in a portion of the asynchronous input data being shifted out of the shift register, the A2S conversion circuitry being operable to discard the portion of the asynchronous input data.

13. The test interface of claim 12 wherein the A2S conversion circuitry is further operable to merge the portion of the asynchronous input data with a remainder of the asynchronous input data for transmission to the first test register.

14. The test interface of claim 10 wherein the shift register is operable to transmit the asynchronous input data in response to a control bit in the asynchronous input data

indicating readiness of an interface associated with the first test register to receive the asynchronous input data.

15. The test interface of claim 10 wherein the shift register is operable to receive the asynchronous output data in response to a control bit in the asynchronous output data indicating validity of the asynchronous output data.

16. The test interface of claim 1 wherein the asynchronous logic is operable to transmit the asynchronous input and output data in accordance with a multi-phase handshake protocol.

17. The test interface of claim 16 wherein the multi-phase handshake protocol between a sender and a receiver in the asynchronous logic comprises:

the sender sets a data signal valid when an enable signal from the receiver goes high;

the receiver lowers the enable signal upon receiving the valid data signal;

the sender sets the data signal neutral upon receiving the low enable signal; and

the receiver raises the enable signal upon receiving the neutral data signal.

18. The test interface of claim 1 wherein the test interface is part of a JTAG compliant interface.

19. The test interface of claim 18 wherein the JTAG compliant interface corresponds to IEEE 1149.1-2001.

20. The test interface of claim 18 wherein the JTAG compliant interface further comprises at least one synchronous register for providing test access to a synchronous circuit associated with the asynchronous circuit.

21. The test interface of claim 20 wherein the at least one synchronous register comprises any of a bypass register, a device identification register, and a boundary scan register.

22. An integrated circuit comprising the test interface of claim 1.

23. The integrated circuit of claim 22 wherein the integrated circuit comprises any of a CMOS integrated circuit, a GaAs integrated circuit, and a SiGe integrated circuit.

24. The integrated circuit of claim 22 wherein the integrated circuit comprises at least one of a programmable logic device, a field-programmable gate array, an application-specific integrated circuit, a microprocessor, and a system on a chip.

25. At least one computer-readable medium having data structures stored therein representative of the test interface of claim 1.

26. The at least one computer-readable medium of claim 25 wherein the data structures comprise a simulatable representation of the test interface.

27. The at least one computer-readable medium of claim 26 wherein the simulatable representation comprises a netlist.

28. The at least one computer-readable medium of claim 25 wherein the data structures comprise a code description of the test interface.

29. The at least one computer-readable medium of claim 28 wherein the code description corresponds to a hardware description language.

30. A set of semiconductor processing masks representative of at least a portion of the test interface of claim 1.

31. A method for testing an asynchronous circuit using synchronous test equipment, comprising:

converting synchronous input data received from the synchronous test equipment to asynchronous input data;

transmitting the asynchronous input data to a first test register in the asynchronous circuit;

receiving asynchronous output data from a second test register in the asynchronous circuit, the asynchronous output data resulting from application of the asynchronous input data to the asynchronous circuit; and

converting the asynchronous output data to synchronous output data; and

serially transmitting the synchronous output data to the synchronous test equipment;

wherein transmission and reception of the asynchronous input and output data are synchronized at least in part with a clock signal associated with the synchronous test equipment.

32. The method of claim 31 wherein transmitting the asynchronous input data to the first test register comprises receiving the asynchronous input data with a shift register, and wherein receiving the asynchronous output data from a second test register comprises receiving the asynchronous output data with the shift register.

33. The method of claim 32 wherein transmitting the asynchronous input data to the first test register further comprises transmitting the asynchronous input data in parallel from the shift register to a parallel-to-serial (P2S) register, and transmitting the asynchronous input data serially from the P2S register to the first test register.

34. The method of claim 33 wherein transmitting the asynchronous input data serially from the P2S register to the first test register is done via a serial tree interface coupled between the P2S register and the first test register.

35. The method of claim 32 wherein receiving the asynchronous output data from a second test register further comprises transmitting the asynchronous output data serially from the second test register to a serial-to-parallel (S2P) register, and transmitting the asynchronous output data in parallel from the S2P register to the shift register.

36. The method of claim 35 wherein transmitting the asynchronous output data serially from the second test register to the S2P register is done via a serial tree interface coupled between the S2P register and the second test register.

37. The method of claim 32 wherein receiving the asynchronous input data with the shift register comprises shifting in the asynchronous input data and shifting out previous asynchronous output data.

38. The method of claim 37 further comprising commencing shifting the previous asynchronous output data out of the shift register before commencement of shifting the asynchronous input data into the shift register.

39. The method of claim 38 wherein commencing shifting of the previous asynchronous output data and subsequent shifting of the asynchronous input data results in a portion of the asynchronous input data being shifted out of the shift register, the method further comprising discarding the portion of the asynchronous input data.

40. The method of claim 39 further comprising merging the portion of the asynchronous input data with a remainder of the asynchronous input data for transmission to the first test register.

41. The method of claim 37 wherein transmitting the asynchronous input data to the first test register is done in response to a control bit in the asynchronous input data indicating readiness of an interface associated with the first test register to receive the asynchronous input data.

42. The method of claim 37 wherein receiving the asynchronous output data from the second test register is done in response to a control bit in the asynchronous output data indicating validity of the asynchronous output data.

43. The method of claim 31 wherein transmitting of the asynchronous input and receiving of the asynchronous output data is done in accordance with a multi-phase handshake protocol.

44. The method of claim 43 wherein the multi-phase handshake protocol between a sender and a receiver comprises:

the sender sets a data signal valid when an enable signal from the receiver goes high;

the receiver lowers the enable signal upon receiving the valid data signal;

the sender sets the data signal neutral upon receiving the low enable signal; and

the receiver raises the enable signal upon receiving the neutral data signal.

45. The method of claim 31 wherein testing of the asynchronous circuit using the synchronous test equipment is done in accordance with a JTAG protocol.

46. The method of claim 45 wherein the JTAG protocol corresponds to IEEE 1149.1-2001.

47. The method of claim 46 further comprising providing at least one synchronous register for facilitating test access to a synchronous circuit associated with the asynchronous circuit.

48. The method of claim 47 wherein the at least one synchronous register comprises any of a bypass register, a device identification register, and a boundary scan register.